Attorney's Docket No.: 042390P16670 Patent

UNITED STATES PATENT APPLICATION

For

METHOD OF FABRICATING A MICROELECTRONIC DIE

Inventor:

Kramadhati V. Ravi

Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CALIFORNIA 90025-1026
(408) 720-8300

Attorney Docket No.: 042390P16670

"Express Mail" mailing label number: EV 336582915 US
Date of Deposit: July 24, 2003
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Linda K. Brost
(Typed or printed name of person mailing paper or fee)

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(Signature of person mailing paper or fee)

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(Date signed)

METHOD OF FABRICATING A MICROELECTRONIC DIE

BACKGROUND OF THE INVENTION

1). Field of the Invention

[0001] This invention relates generally to a method of fabricating a microelectronic die, and more specifically to a method for increasing electron mobility values of channel regions of semiconductor transistors.

2). Discussion of Related Art

[0002] Transistors that make up integrated circuits of microelectronic dies are manufactured in and on silicon or other semiconductor substrates. Such a transistor has a channel region and source and drain regions on opposing sides of the channel region. The transistor further has a gate dielectric layer and a gate electrode which are formed on the channel region. A voltage that switches on the gate electrode can switch a current that flows between the source and drain regions through the channel region.

[0003] It has been recognized that a large tensile stress can increase both electron mobility of N-MOS devices and hole mobility of P-MOS devices. Several approaches to inducing strain in silicon have been proposed, including mechanical deformation of silicon wafers, local stressing of devices with thermal-expansion mismatched films, and the use of graded layer epitaxy of silicon germanium (SiGe)

films on silicon followed by silicon epitaxy on the relaxed SiGe. The degree of stress that can be provided by these processes is usually relatively limited, which, when making a C-MOS wafer, necessitates that a tensile stress be provided for an N-MOS device and a compressive stress for a P-MOS device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The invention is described by way of example with reference to the accompanying drawings, wherein:

[0005] Figure 1 is a side view representing a high-quality silicon handle substrate;

[0006] Figure 2 is a view similar to Figure 1 after the formation of a diamond intermediate substrate on the handle substrate, and subsequent cooling of the combination;

[0007] Figure 3 is a graph of coefficients of thermal expansion (CTEs) of silicon and diamond at different temperatures;

[0008] Figure 4 is a view similar to Figure 3 after a compensating polysilicon layer is formed to counteract bowing induced due to the process resulting in the structure of Figure 2;

[0009] Figure 5 is a graph representing a compensating bow as a function of deposition temperatures of the compensating polysilicon layer;

[0010] Figure 6 is a view similar to Figure 4 after a monocrystalline silicon layer is formed on the structure of Figure 4;

[0011] Figure 7 is a side view illustrating a transistor and other portions of an integrated circuit that are formed in and on the monocrystalline silicon layer;

[0012] Figure 8 is a plan view illustrating a combination wafer of Figure 6 with a plurality of integrated circuits formed in rows and columns thereon;

[0013] Figure 9 is a view similar to Figure 6 after the handle substrate is removed to increase bowing of the resulting combination wafer and induce a stress in the

monocrystalline silicon film; and

[0014] Figure 10 is a view similar to Figure 7, illustrating the stress in a channel of one of the transistors.

DETAILED DESCRIPTION OF THE INVENTION

[0015] A method of fabricating a microelectronic die is provided. Transistors are formed in and on a semiconductor layer. A channel of each transistor is stressed after the transistors are manufactured by first forming a diamond intermediate substrate at an elevated temperature on a handle substrate, allowing the intermediate substrate and the handle substrate to cool, attaching the semiconductor layer, and then removing the handle substrate. The intermediate substrate has a lower CTE than the handle substrate, so that the intermediate substrate tends to bow when the handle substrate is removed. Such bowing creates a tensile stress, which translates into a biaxial strain in channel regions of the transistors. Excessive bowing is counteracted with a compensating polysilicon layer formed at an elevated temperature and having a higher CTE on a side of the diamond intermediate substrate.

[0016] As illustrated in Figure 1, the method of fabricating a microelectronic die, according to an embodiment of the invention, is initiated with a handle substrate 10. The handle substrate 10 is preferably a silicon substrate. One reason why a silicon substrate is preferred is because existing techniques allow for silicon substrates to be manufactured to a high degree of flatness. A further reason why silicon is preferred is because of the ability to deposit polysilicon thereon. Silicon is also a preferred substrate to be used in wafer manufacturing equipment, because such equipment is usually adjusted for the known responses of silicon to various thermal and chemical conditions.

[0017] As illustrated in Figure 2, a diamond intermediate substrate 12 is subsequently formed on the handle substrate 10. The combination of the handle substrate 10 and the intermediate substrate 12 forms a first combination wafer 14. The intermediate substrate 12 is formed at an elevated temperature and has a lower CTE than the handle substrate 10, so that subsequently cooling of the combination wafer 14 results in more contraction of the handle substrate 10 than the intermediate substrate 12. The combination wafer 14 bows into a first shape due to the differential CTEs of the handle substrate 10 and the intermediate substrate 12. The combination wafer 14 may bow by a depth 16 of between 200 and 300 microns, if the combination wafer 14 has a diameter of about 200 mm.

[0018] As illustrated in Figure 3, diamond has a CTE below that of silicon at all temperatures below approximately 1080 K. In the present example, therefore, the diamond is preferably formed at a temperature below 1000°C. The depth 16 can be controlled by adjusting the deposition temperature of the diamond.

[0019] As illustrated in Figure 4, a polysilicon compensating layer 18 is subsequently formed on all surfaces of the first combination wafer 14 to form a second combination wafer 19. The compensating layer 18 grows differently on the diamond of the intermediate substrate 12 and the silicon of the handle substrate 10, so that the compensating layer 18 has a higher CTE on the intermediate substrate 12 on the handle substrate 10. The compensating layer 18 is formed at an elevated temperature. Subsequent cooling of the compensating layer 18, together with the combination wafer 14, causes faster contraction of the compensating layer 18 on the

intermediate substrate 12 and on the handle substrate 10, so that the combination wafer 14 is bent in an opposite direction that tends to return the handle substrate 10 to its shape in Figure 1. The second combination wafer 19 then has a second shape with a bow having a depth 20 of approximately 5 microns, but the depth 20 could be as low as zero microns.

[0020] As illustrated in Figure 5, the degree to which the polysilicon compensating layer 18 returns the combination wafer 14 to its original shape (i.e., the difference between the depth 16 in Figure 2 and the depth 20 in Figure 4) depends on the deposition temperature of the polysilicon compensating layer 18. Lower deposition temperatures return the combination wafer 14 to its original shape more than higher deposition temperatures. A deposition temperature of 600°C may create a compensating bow of 300 microns, whereas a deposition temperature of 1000°C will only create a compensating bow of 5 microns. In the case where the original bow has a depth 16 of 200 microns, a polysilicon deposition temperature of 700° will create a compensating bow of 200 microns, so that the depth 20 is zero.

[0021] Referring now to Figure 6, a monocrystalline silicon (semiconductor) layer 22 is subsequently formed on an upper surface of the compensating layer 18, and is thereby connected through the compensating layer 18 to the intermediate layer 12. The monocrystalline silicon layer 22, for example, may be formed by attaching a wafer substrate to the compensating layer 18, and then grinding the wafer substrate back to a desired thickness to form a final combination wafer 24. The final combination wafer 24 typically has a monocrystalline silicon handle substrate 10

having a thickness of 500 to 650 microns, a diamond intermediate substrate 12 having a thickness of between 50 and 200 microns, and a monocrystalline silicon layer 22 having a thickness of approximately 2 microns with a tolerance of approximately 0.5 microns.

[0022] As illustrated in Figure 7, a plurality of transistors 28, one of which is shown, are subsequently formed in and on the monocrystalline silicon layer 22. The monocrystalline silicon layer 22 is P-doped, so that each transistor 28 has a channel 30 which is P-doped. N-doped source and drain regions 32 are formed by implanting impurities on opposing sides of the channel 30. Each transistor 28 further has a gate dielectric layer 34 formed on the channel 30, and a conductive gate electrode 36 on the gate dielectric layer 34. Further aspects of the manufacture of transistors are known in the art, and are not discussed in detail herein. As will also be understood in the art, non-conductive dielectric layers are subsequently formed over the monocrystalline silicon substrate layer 22 and the transistors 28 with conductive vias and metal lines 40 that interconnect the transistors 28 and other components to create an integrated circuit. What should be noted is that the channels 30 of the transistors 28 are at this stage not stressed.

[0023] As illustrated in Figure 8, the combination wafer 24 has a plurality of such integrated circuits 42. The integrated circuits 42 are identical to one another, and are replicated in rows and columns over the combination wafer 24.

[0024] Reference is now made to Figure 9. As illustrated, the handle substrate 10 of Figure 6 is removed, together with the portions of the compensating layer 18

formed thereon. The handle substrate 10 may, for example, be removed in a grinding operation. Removal of the handle substrate 10 causes bowing of the remaining combination wafer 43 to a depth 44 of between 10 and 20 microns. Referring again to Figure 2, the bowing of the combination wafer 14 is a balance struck between the tendency for the intermediate substrate 12 to create bowing of the combination wafer 14 and the tendency of the handle substrate 10 to resist any such bowing. Removal of the handle substrate 10, as illustrated in Figure 9, thus removes the tendency for the handle substrate to resist bowing, and the tendency for the intermediate substrate 12 to bow then dominates. The tendency for the intermediate substrate 12 to bow is still counteracted, to an extent, by the compensating layer 18, so that the depth 44 of Figure 9 is less than the depth 16 of Figure 2. The effect of the bowing of the combination wafer 43 is that a tensile stress 50 is created in the monocrystalline silicon layer 22.

[0025] As illustrated in Figure 10, the tensile stress 50 is in the channel 30 of each transistor 28. The stress in the channel 30 induces a strain in the channel 30. The strain-induced band structure modification and the mobility enhancement of silicon increases drive currents. The strain removes electron band degeneracy and produces energy shifts in the conduction and valence bands. It has been found that higher carrier mobility can be achieved by inducing biaxial tensile strain in thin (100) silicon films. In the present example, it has been shown that electron mobility values are increased from 1600 cm^2/Vs to about 2300 cm^2/Vs for about a 1% biaxial tensile strain in silicon (M.V. Fischetti and S.E. Laux, *Band Structure, deformation*

potentials, and carrier mobility in strained Si, Ge, and SiGe alloys, J. Appl. Phys. 80, 2234, 1996). A rough order of magnitude calculation of strain that can be introduced in the silicon as a result of differences in the CTE between diamond and silicon indicates that strain levels from about 0.8% to greater than 10% can be achieved over a diamond deposition temperature in the range of 600 to 1000°C.

[0026] An advantage of the process as described is that strained silicon on diamond wafers would be stable at elevated temperatures, as compared with SiGe-based materials. No diffusion or stress relaxation are expected at elevated temperatures (e.g., above 1000°C). A further advantage is that the thickness of the monocrystalline silicon layer 22 can be varied over a broad range, increasing design options compared with SiGe-based materials. A further advantage is that there will be no misfit dislocations in the structures as described, since diamond deposition does not involve epitaxy required in SiGe-based processes. The silicon layer quality will thus be high. Furthermore, conduction band energy band-splitting occurs due to biaxial tensile strain, leading to enhanced electron mobility. It has been found that compared to the conduction band, larger strain is required to induce a given splitting in the balance band. Larger strain in the silicon can be introduced with a silicon-on-diamond structure as described than with strained silicon on relaxed SiGe, thus opening up the possibility for both electron and whole mobility enhancement with large biaxial tensile strain in the silicon. The presence of the diamond film beneath the silicon, due to the exceptional thermal conductivity of diamond, has the additional important advantage of spreading heat from hot spots

in the circuit during device operation.

[0027] The combination wafer 43 is subsequently singulated into individual dies, wherein the transistors in each die are stressed. Referring to Figure 8, each die includes a respective one of the circuits 42. The dies may then be packaged according to known methods.

[0028] While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described since modifications may occur to those ordinarily skilled in the art.